WHAT IS CLAIMED IS:

1. A deblocking filtering apparatus comprising:

a D mode operation circuit for performing a D mode operation for a deblocking filter defined in MPEG-4;

a T mode operation circuit for performing a T mode operation;

an operation mode determination circuit for employing a change in a pixel value near a block boundary to adaptively determine whether the D mode operation or the T mode operation should be performed; and

a selector for selecting either the output of the D mode operation circuit or the output of the T mode operation circuit, in accordance with the output of the operation mode determination circuit,

wherein the D mode operation circuit, the T mode operation circuit and the operation mode determination circuit are operated in parallel in synchronization with the input timings of pixel values that are sequentially input.

2. A deblocking filtering apparatus according to claim 1, wherein the operation mode determination circuit performs a process before, in a time series, the processes for the D mode operation circuit and the T mode operation circuit, selects either the D mode operation circuit or the T mode

operation circuit as an adaptive operation circuit, and transmits a fixed value, instead of an input pixel value, to a non-adaptive operation circuit.

3. A deblocking filtering apparatus according to claim 1,

wherein the D mode operation circuit includes:

a shift register group for shifting an input pixel value;

a first absolute differential value operation circuit for obtaining an absolute differential value for a difference between adjacent registers of the shift register group;

a first comparator for comparing the output of the first absolute differential value operation circuit with a first threshold value;

a first selector for selecting a specific register output by the shift register group in accordance with the output of the first comparator;

a sequence counter for counting the number of cycles following the initiation of the operation;

first and second registers, for holding the output of the first selector for a specific cycle indicated by the sequence counter;

a selector group for changing between the

specific register output of the shift register group and output of the first and the second register in accordance with a cycle indicated by the sequence counter;

a first shifter group for shifting the output of the selector group to the left;

a first adder group for adding the output of the selector group and the output of the first shifter group;

a first shifter for shifting the output of the first adder group to the right;

third and fourth registers for holding the maximum value and the minimum value for the specific register output of the shift register group during a specific cycle indicated by the sequence counter;

a second absolute differential value operation circuit for obtaining an absolute differential value for a difference between the third and the fourth registers;

a second comparator for comparing the output of the second absolute differential value operation circuit with a second threshold value; and

a second selector, for changing the specific register output of the shift register group and the output of the first shifter in accordance with the

output of the second comparator,

wherein the T mode operation circuit includes:

a second shifter group for shifting to the left the specific register output of the shift register group;

a second adder group for adding the specific register output of the shift register group and the output of the second shifter group;

a second shifter for shifting the output of the second adder group to the right;

an adder for adding the output of the second shifter to the specific register output of the shift register group;

a subtracter for subtracting the output of the second shifter from the specific register output of the shift register group;

a third comparator for comparing the absolute value for the output of the second shifter with a third threshold value; and

a third selector for switching the specific register output of the shift register group, the output of the adder and the output of the subtracter in accordance with the output of the third comparator,

wherein the operation mode determination circuit includes:

a third absolute differential value operation circuit for obtaining an absolute differential value for a difference between adjacent registers in the shift register group;

a fourth comparator for comparing the output of the third absolute differential value operation circuit with a fourth threshold value;

a counter for cumulatively adding the output of the fourth comparator; and

a fifth comparator, for comparing the output of the counter with a fifth threshold value,

wherein the selector switches the output of the D mode operation circuit and the output of the T mode operation circuit in accordance with the output of the operation mode determination circuit.

4. A deblocking filtering method comprising:

a D mode operation step of performing a D mode operation for a deblocking filter defined in MPEG-4;

a T mode operation step of performing a T mode operation;

an operation mode determination step of employing a change in a pixel value near a block boundary to adaptively determine whether the D mode operation or the T mode operation should be performed; and

a step of selecting either the output at the D mode operation

step or the output at the T mode operation step in accordance with the output at the operation mode determination step,

wherein the D mode operation, the T mode operation and the operation mode determination are performed in parallel in synchronization with the input timings for pixel values that are sequentially input.

5. A deblocking filtering method according to claim 4, wherein the operation mode determination is performed before, in a time series, the D mode operation and the T mode operation are initiated, either the D mode operation or the T mode operation is determined as an adaptive operation, and a fixed value, rather than an input pixel value, is input as a non-adaptive operation.